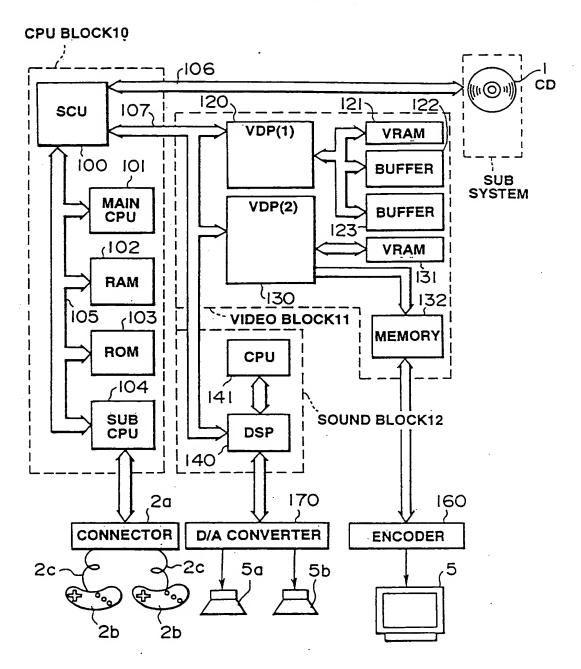
4639

FIG.1



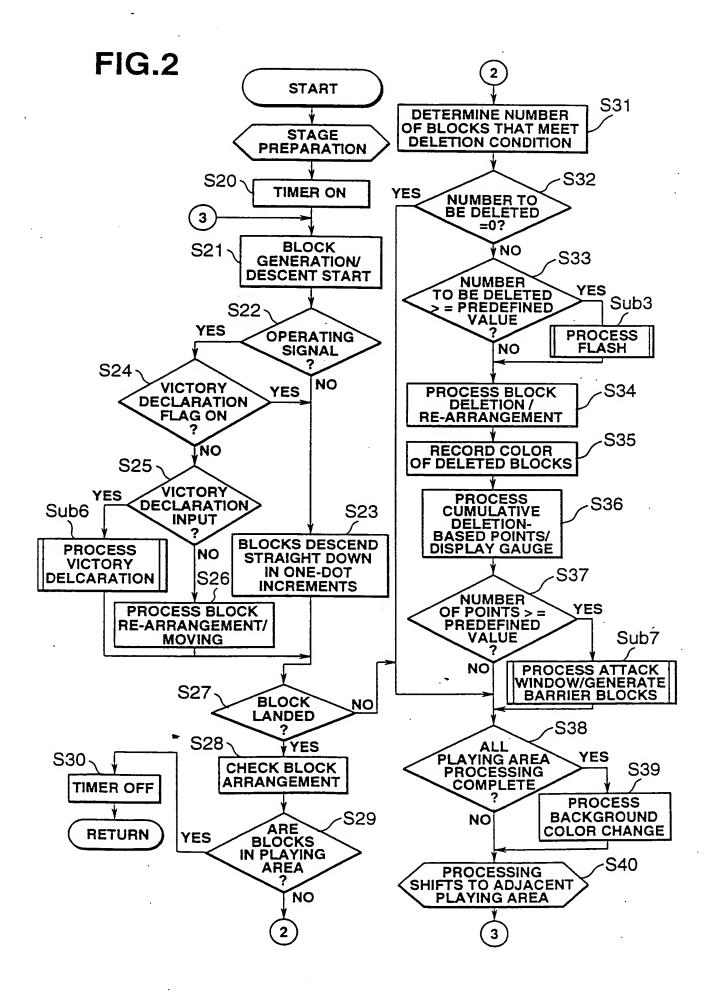


FIG.3A

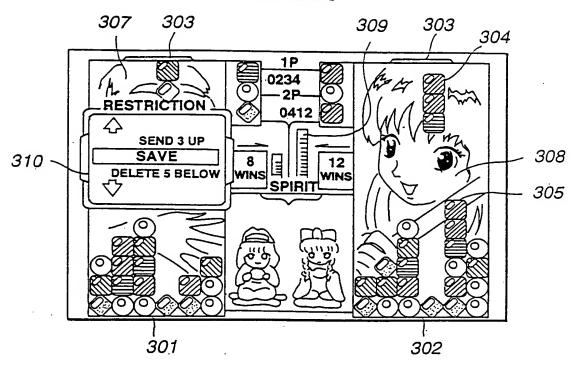


FIG.3B

FIG.3C

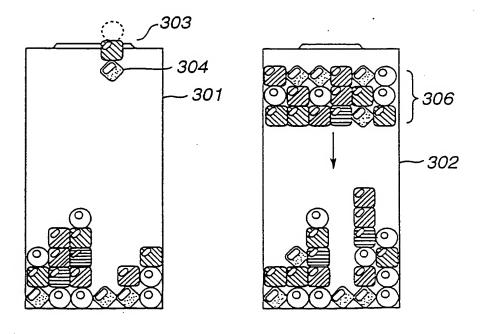
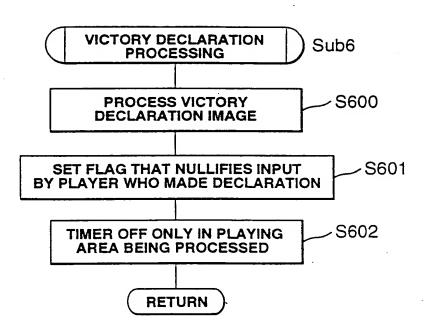
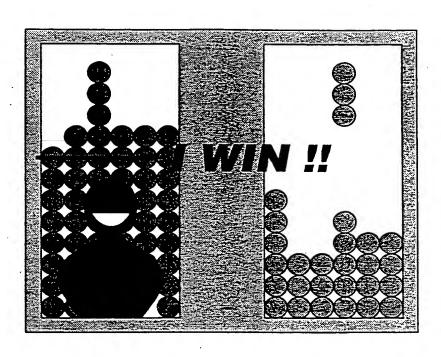
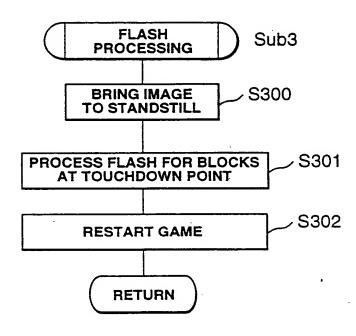
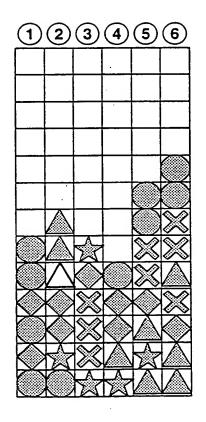


FIG.4









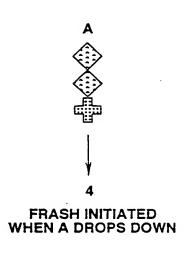


FIG.8

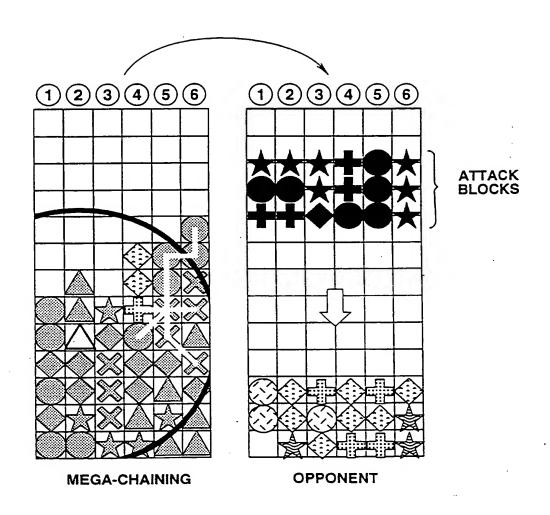
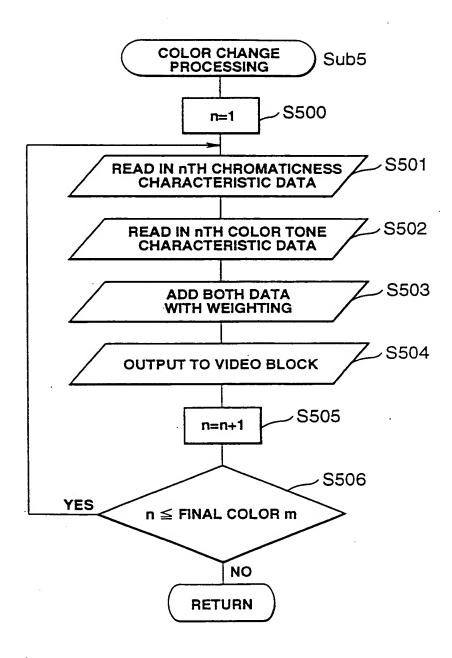
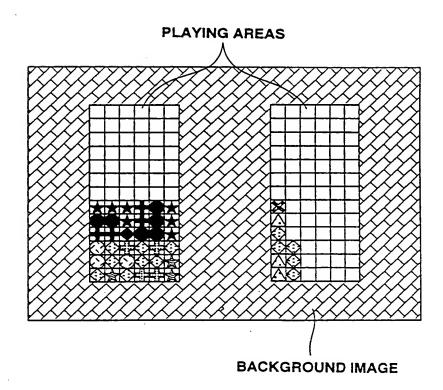
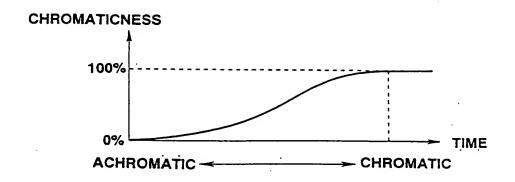


FIG.9





**FIG.11** 



**FIG.12** 

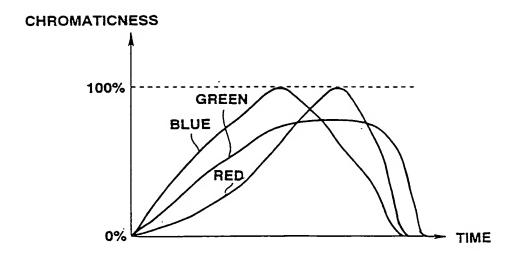
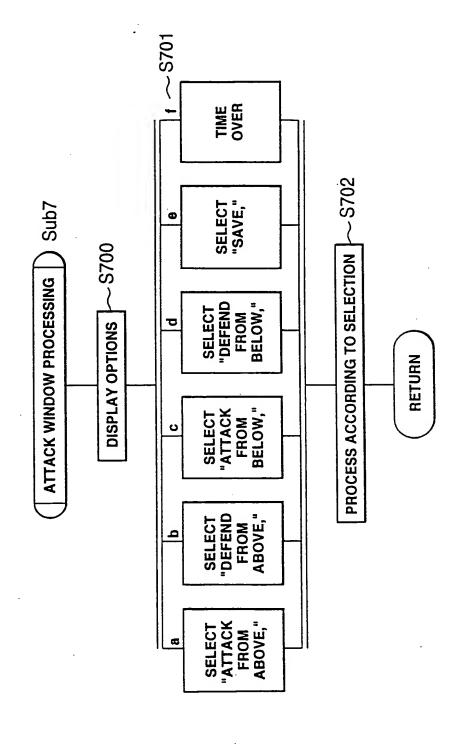
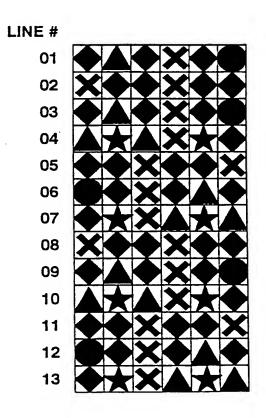
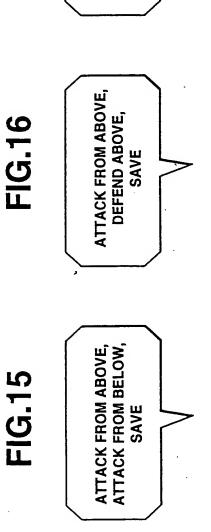
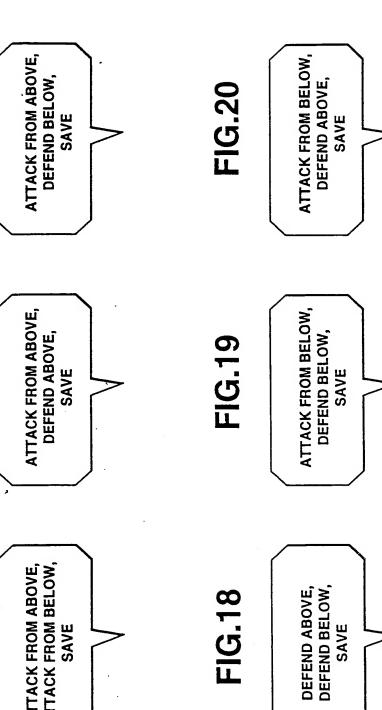


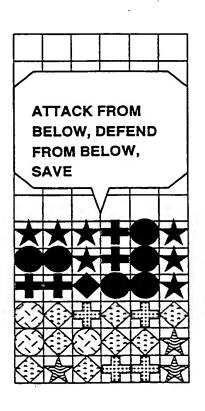
FIG.13

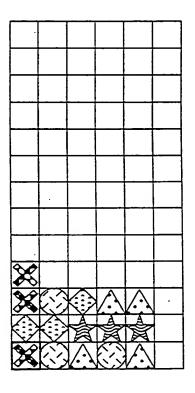




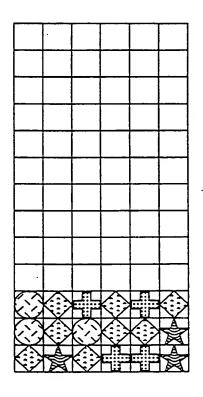


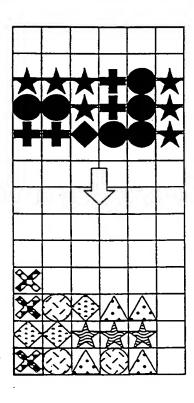




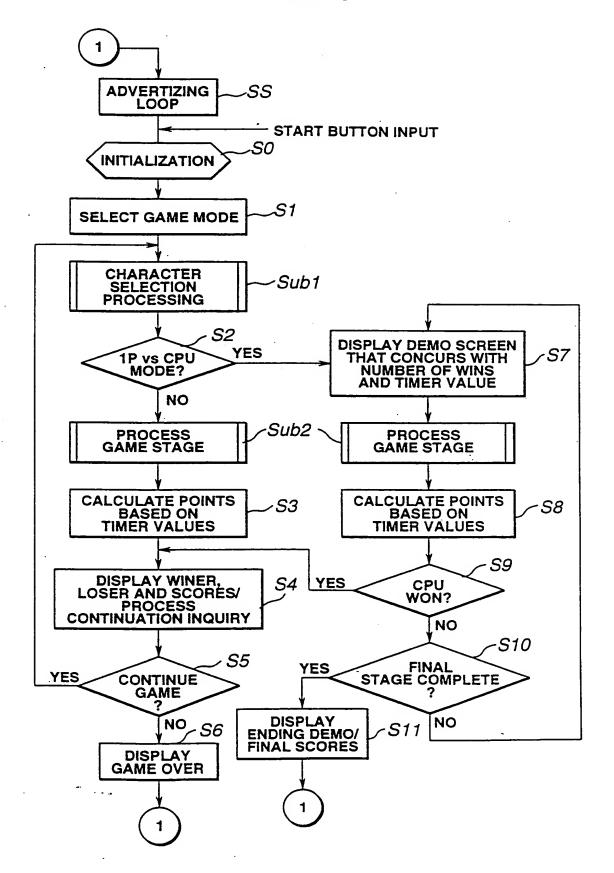


**FIG.22** 

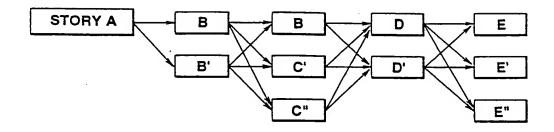




**FIG.23** 



**FIG.24** 



**FIG.25** 

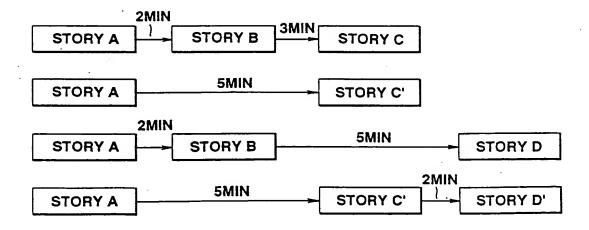
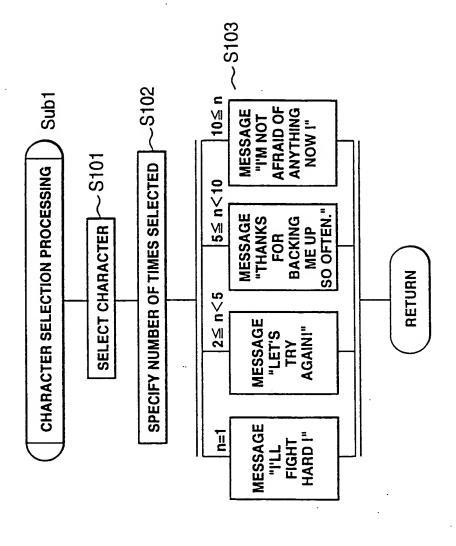
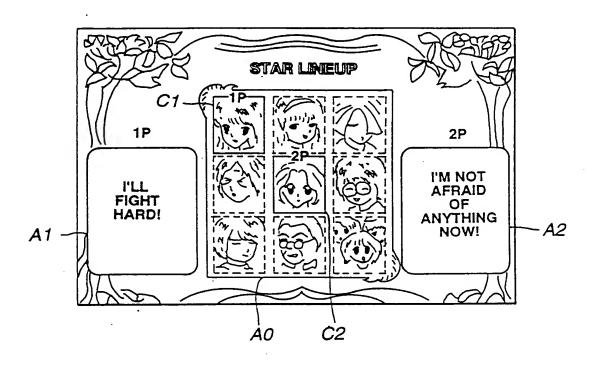
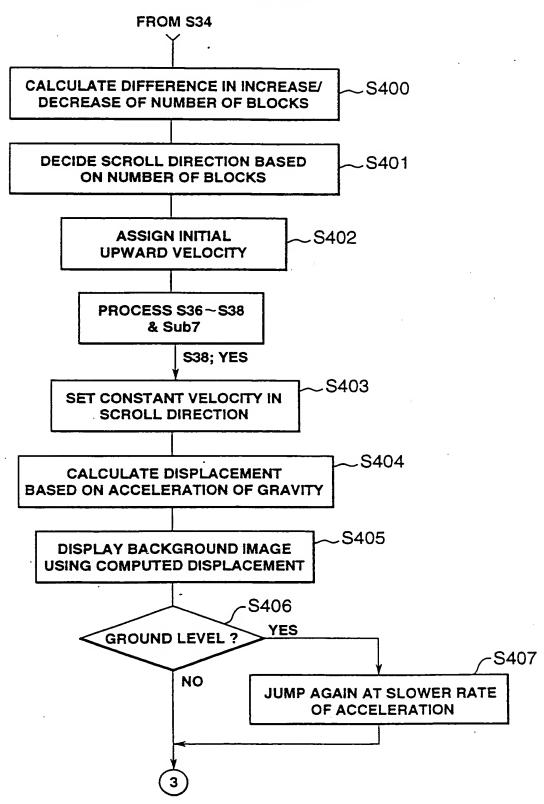


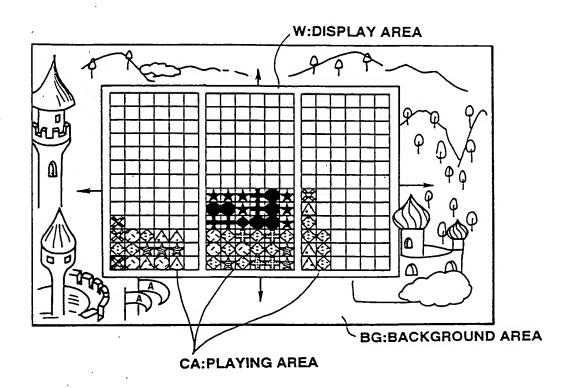
FIG.26



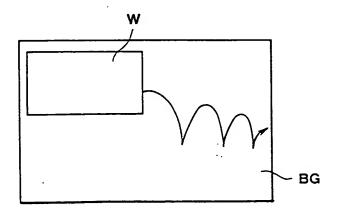


**FIG.28** 





**FIG.30** 



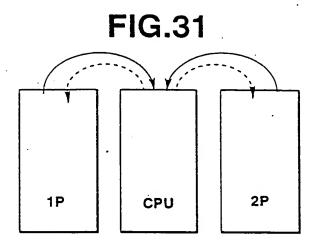
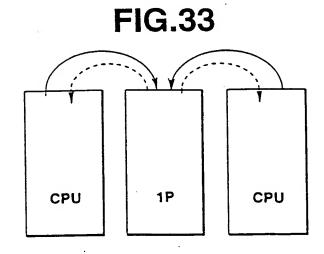


FIG.32

1P CPU 2P



**FIG.34** 

